

REMARKS

This paper responds to the Office Action mailed on May 27, 2008.

Claims 1, 8 and 9 are amended, claims 11-19 are canceled without prejudice or disclaimer, and claim 31 is added; as a result, claims 1, 3-10, and 20-31 are now pending in this application. Claims 20-30 currently stand withdrawn. Applicant respectfully submits that the claim amendments contained herein present no new matter and find support in the specification.

The subject matter of claims 11-19 were filed in a divisional application (11/354,443), which issued as patent no. 7,402,482.

§102 Rejection of the Claims

Claims 1, 3-4, 6 and 9-10 were rejected under 35 U.S.C. § 102(e) for anticipation by Lee et al. (U.S. Patent No. 6,687,157). Applicant respectfully traverses this rejection.

The cited reference of Lee discloses forming a 2T cell having a Flash transistor and a mask ROM transistor (abstract; figures 4, 7A-D; col. 4, lines 1-10; col. 6, lines 11-22). Lee discloses an embodiment having the ROM transistor formed by shorting the floating gate to the control gate, which the Examiner states on page 3 to mean that “the two cells inherently have the same footprint and the same area footprint”. Applicant can find no disclosure or suggestion in Lee of any motivation to form the Flash and mask ROM transistors with the same footprint. The present claims, as amended herein, recite that the ROM transistor has a single conductive layer electrode in the read-only memory transistors, which is clearly different than the cited reference teachings and Applicant asserts the claim to be patentably distinct over Lee, which does not teach or suggest any motivation to have the Flash and mask ROM transistors formed with the same footprint.

Applicant respectfully submits that the cited reference fails to disclose at least the feature of a “...mask programmed single conductive layer electrode read-only memory ...”, as recited in independent claim 1, as amended herein. Lee does not disclose either the single conductive layer electrode in the sections cited by the Examiner, or any suggestion of motivation for forming the ROM transistor cells with the same footprint as the non-volatile user programmable memory transistor cells. Thus Lee does not disclose each and every claimed feature of the present claims.

Applicant submits that the dependent claims are held to be patentable at least as depending from an allowable base claim. Applicant respectfully requests that this rejection under 35 U.S.C. § 102(e) be reconsidered and withdrawn.

§103 Rejection of the Claims

Claims 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 6,687,154). Applicant respectfully traverses this rejection.

The single cited reference of Lee has features discussed above with respect to the prior rejection, and Lee does not describe or suggest a single conductive layer electrode when forming the ROM transistor cells with the same footprint as the non-volatile user programmable memory transistor cells.

Applicant respectfully submits that the cited reference fails to describe or suggest at least the claimed feature of a “...mask programmed single conductive layer electrode read-only memory ...”, as recited in amended independent claim 1, from which claims 7 and 8 depend. The reasoning is similar to that given above with reference to the prior rejection, specifically that there is no suggestion of wanting to have the two different transistors have the same footprint, and that the ROM transistors have a single conductive layer for the electrode. Lee suggests that the ROM have a two layer electrode. Thus base claim 1 is non-obvious over Lee.

The dependent claims are asserted to be patentable at least as depending from a base claim shown above to be patentable over the cited reference, whether taken alone or in any combination with other well known art, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the above noted claim amendments and discussion of the failure of the cited references to describe or suggest at least the above features, Applicant requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 6,687,154) in view of Hsu et al. (U.S. Patent No. 6,822,286). Applicant respectfully traverses this rejection.

Lee has been discussed above. Hsu is used in the outstanding Office Action to show that it is known to use “one poly layer” for the ROM. Applicant submits that Hsu does not cure the previously discussed failure of Lee to suggest that the non volatile and ROM transistors have the same footprint. Applicant further submits that the suggested combination has no motivation to make the proposed combination, and the Examiner merely makes the conclusory statement that it would have been obvious to one of ordinary skill in the art “to incorporate the feature, as taught by Hsu, into the Lee 154 device and come up with the invention of claim 5”. Applicant submits that Lee teaches the benefits of using two poly layers at the location indicated by the Examiner (i.e., figure 7B and col. 13, lines 13-25) where it states “By modifying a Flash cell into a mask ROM cell, both devices rely on the same process and the fabrication is simplified”. Thus the Examiner’s proposed combination of references tend to teach away from each other, and thus proper motivation does not exist to make the proposed combination of references.

Specifically, Applicant respectfully submits that the cited reference fails to describe or suggest at least the feature of a “*...mask programmed single conductive layer electrode read-only memory ...*”, as recited in independent claim 1, as amended herein, from which claim 5 depends. There exists no possible motivation for one of ordinary skill in the art to combine a reference teaching the benefits of two poly layers with a reference teaching a single poly layer, and further neither reference suggests a non volatile transistor should have the same footprint as a ROM transistor. Thus, even if there were proper motivation to make the proposed combination, the result would still not contain each and every claimed feature.

The dependent claim is held to be patentable at least as depending from a patentable base claim as shown above, since any claim depending from a nonobvious independent claim is also nonobvious. See M.P.E.P. § 2143.03. In view of the above noted claim amendments and discussion of the failure of the cited references to describe or suggest at least the above features, Applicant requests this rejection under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have equally addressed every assertion made in the Office Action, however, this does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10810,035

Filing Date: March 26, 2004

Title: Non-volatile transistor memory array incorporating read-only elements with single mask set

Page 9
Dkt: 2800.450US1

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

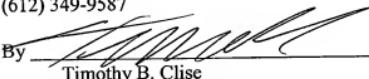
Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date

29 Sept 108

By


Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 29 day of September 2008.

Name

Nicole Jan

Signature

